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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,327	04/28/2004	David J. Hathaway	BUR920030176US1	3326

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EXAMINER
BOWERS, BRANDON

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
10/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,327	HATHAWAY ET AL.	
	Examiner	Art Unit	
	Brandon W. Bowers	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,15,16 and 21* is/are rejected.

7)☒ Claim(s) *5-14 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20040428, 20040722*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,15-16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bull, US Patent No. 5,655,107 in view of Chang et al. US Patent No. 6,415,426.

In reference to claims 1 and 21, Bull teaches a digital logic wire delay simulation method that includes partitioning timing delays in a digital network into portions attributable to a factor of interest and portions attributable to other factors (wire delays and non-wire delays, column 19, lines 44 – 56). Bull does not teach multiplying the timing delays by different weights and using the multiplied timing delays to determine delay impact of the factor of interest on the paths in the digital network. Chang teaches multiplying timing delays by different weights and using the multiplied timing delays to determine delay impact on the paths in the digital network (Figure 2, 52 and 58, and column 7, lines 1-35). Accordingly it would have been obvious for one skilled in the art at the time of invention to incorporate the teaches of Bull into the teachings of Chang to create a method comprising all of the limitations as taught in claim 1 because it would provide a logic simulation system that supports wire delays that accurately reflect values

of the logic circuit being modeled without incurring a significant performance penalty (Bull, column 2, lines 13-17).

In reference to claim 2, Bull teaches identifying paths whose delays are dominated by the factor of interest (wire delays and non-wire delays, column 19, lines 44 – 56).

In reference to claim 3, Chang teaches wherein the arrival times of the timing signals start at zero (column 9, lines 48-57).

In reference to claim 4, Chang teaches wherein the weights can be positive negative or zero (column 22, lines 46-59).

In reference to claim 15, Bull teaches a digital logic wire delay simulation method that includes categorizing factors that influence signal timing delays in a digital network into portions attributable to a factor of interest and portions attributable to other factors and determining paths whose delays are dominated by the factor of interest (wire delays and non-wire delays, column 19, lines 44 – 56). Bull does not teach attributing different weights based on the categorization. Chang teaches attributing different weights based upon timing delays categorizations (Figure 2, 52 and 58, and column 7, lines 1-35). Accordingly it would have been obvious for one skilled in the art at the time of invention to incorporate the teaches of Bull into the teachings of Chang to create a method comprising all of the limitations as taught in claim 1 because it would provide a logic simulation system that supports wire delays that accurately reflect values of the logic circuit being modeled without incurring a significant performance penalty (Bull, column 2, lines 13-17).

In reference to claim 16, Chang teaches wherein the weights can be positive negative or zero (column 22, lines 46-59).

Allowable Subject Matter

Claims 5-14 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W. Bowers whose telephone number is (571)272-1888. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571)272-7483.. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BWB

JACK CHIANG
SUPERVISORY PATENT EXAMINER